Application No.: 09/752,122   Docket No.: JCLA6705

In The Abstract:

Please substitute Abstract as follows :

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[A memory data access structure and an access method suitable for use in a processor. For each instruction executed by the processor, the execution results are recognized by the processor and transferred to a cache memory via control signals. When the instruction to be fetched is not stored in the cache memory, according to the control signals, the cache memory can determine whether the instruction is to be fetched from an external memory. With such structure, no matter whether the processor comprises a branch prediction mechanism or not, many operation clock cycles consumed in the processor of the prior art are saved by compensating for the situation that the cache memory fails to fetch, that is, a Miss of the cache memory. The efficiency and performance of the processor can be effectively enhanced.]

A memory data access structure and method in a processor is provided. The structure comprises a cache memory and a pipeline processor. The cache memory is used to store and output an instruction according to an address signal. The pipeline processor is used for executing a plurality of processor instructions, the pipeline processor including an execution unit to perform an execution operation on the instruction input from a previous stage, and to output a result signal and a control signal, wherein the control signal is output to the cache memory. When the instruction executed by the execution unit is a branch instruction, the result signal is a target address. The target address is selected to be an address signal output to the cache memory. The cache memory fetches a next instruction to be executed according to the

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address signal.   When the execution unit is executing the branch instruction, the processor is fetching a fetch instruction from the cache memory, and when the control signal obtained after executing the branch instruction is output to the cache memory, if the fetch instruction is not stored in the cache memory, the cache memory determines whether to fetch the fetch instruction from an external memory according to the control signal.

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